Analyzing Super-Junction C-V to Estimate Charge Imbalance

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***Abstract*—In this paper, we present a new technique to model charge imbalance in Super Junction devices using junction (Drain-Source for MOSFET) C-V measurements. In contrast to Breakdown Voltage measurement that can also be used for this purpose, this technique offers significant advantages by having no dependence on the edge termination BV for its accuracy. In addition, this method can be used to estimate both the magnitude (δQ) and polarity ($Q_P>Q_N$ or $Q_P<Q_N$) of charge imbalance**

I. INTRODUCTION

Super Junction devices achieve significant reduction in the specific on resistance ($R_{DS}.A$) of high voltage MOSFETs by de-coupling the inverse relationship between parallel plane breakdown voltage (BV_{PP}) and the drift region doping [1]. This fundamental breakthrough is achieved by introducing a P column in the drift region [2] to compensate the N conduction region charge, thereby achieving an ideal rectangular electric field profile. As a result the BV of a Super Junction drift region does not depend on the doping of the N region, but instead on the net charge that is the difference between the P column charge (Q_P) and the N column charge (Q_N). References [3, 4] analyze the effect of charge imbalance on the breakdown voltage of Super Junction.

In addition to breakdown voltage, the avalanche current handling capability during un-clamped inductive load switching (UIS) has also been found to have a strong dependence on the column charge imbalance, as reported in [5]. A P charge heavy ($Q_P>Q_N$) has a much higher UIS capability compared to a charge balanced/N charge heavy Super Junction ($Q_P<Q_N$). From the above discussion, it is clear that the magnitude and polarity of charge imbalance between the P and N columns of Super Junction devices is an important parameter for Super Junction devices that determines its BV and UIS characteristics.

In this work, we propose a novel technique to estimate the charge imbalance between the P and N columns in a Super Junction device based on the measurement of its Pinch off Voltage V_{Pinch} and zero bias junction capacitance C_{J0}. Any method of estimating the charge imbalance based on measuring the BV will work only if the device BV is limited by the cell breakdown. Ensuring a termination BV higher than cell BV throughout the process window of a super junction device is costly and difficult to achieve. Also, BV measurement by itself cannot be used to determine the polarity of charge imbalance, and requires destructive tests such as UIS. The proposed method on the other hand is an easy, non-destructive method that has no dependence on the edge termination design/BV, and can estimate the magnitude and polarity of charge imbalance. Estimation of column charge imbalance from wafer level CV measurements can be used to explain device characteristics, and also be used to tune the fabrication process.

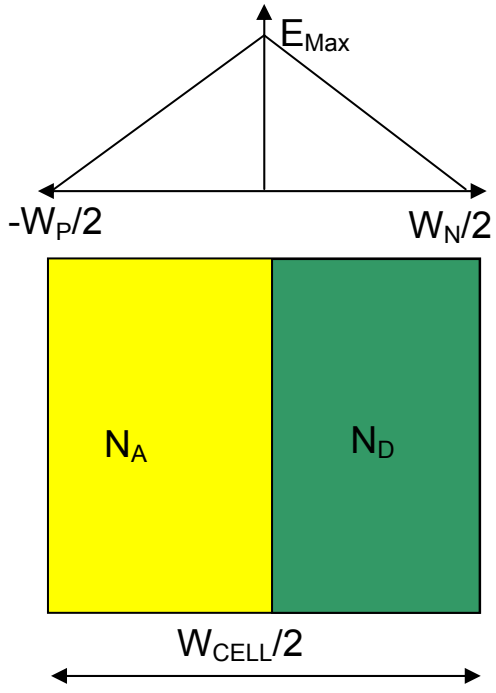
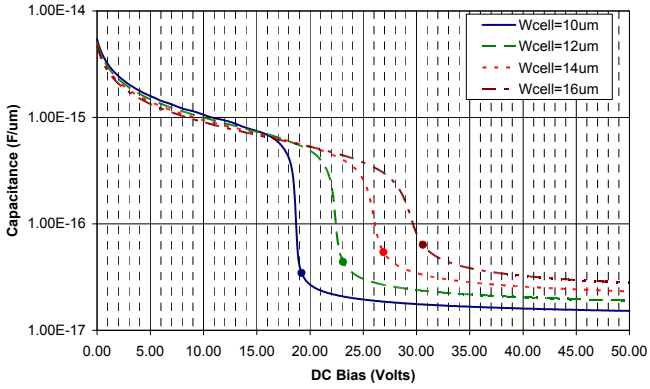
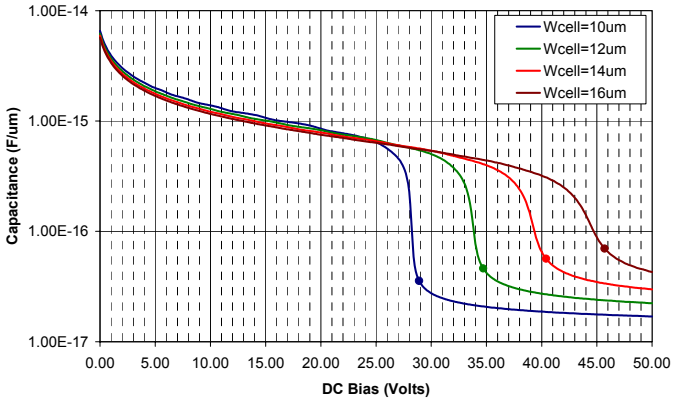


Figure 1. Electric field profile for perfectly charge balanced Super Junction Columns at Pinch-off



A.



B.

Figure 2. Simulated Drain-Source C-V curve for Column Charge Q=1e12.cm^{-2} (A) and Q=1.5e12.cm^{-2} (B)

II. ANLYTICAL MODEL AND SIMULATION RESULTS

A. Charge Balanced Super Junction Columns

A typical drain-source Capacitance-Voltage (CV) curve of a Super Junction shows a sharp drop in the capacitance when the P and N columns deplete each other. This usually happens at low drain biases at which the electric field can be approximated to be horizontal. The voltage at which this sharp drop in capacitance happens is defined as the pinch off voltage (V_{Pinch}). Figure 1 shows the electric field profile for a perfectly charge balanced Super Junction at pinch-off. The analytical expression for the pinch off voltage can be derived as follows:

$$V_{Pinch} = 0.5 * E_{Max} * \left(\frac{W_N}{2} + \frac{W_P}{2} \right) \quad (1)$$

$$E_{Max} = \frac{q}{\varepsilon_s} * N_A * \frac{W_P}{2} = \frac{q}{\varepsilon_s} * N_D * \frac{W_N}{2} = \frac{q * Q_N}{2 * \varepsilon_s} \quad (2)$$

Substituting in (1),

$$V_{Pinch} = \frac{q * Q_N * W_{Cell}}{8 * \varepsilon_s} \quad (3)$$

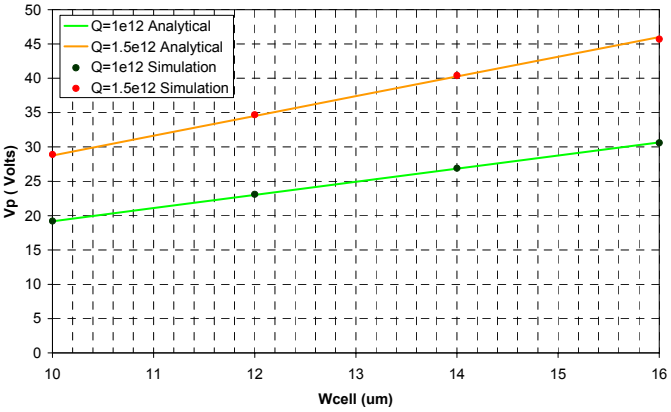


Figure 3. Comparison of Analytical & Simulated V_{Pinch} for different Cell Pitch (W_{CELL}) and column charge (Q)

where W_{Cell} is the total cell pitch. Thus, the pinch off voltage of a Super Junction is directly proportional to its column charge and its cell pitch. Figures 2A and 2B show the simulated CV curve for charge balanced Super Junction with Q_P=Q_N= 1e12.cm^{-2} and 1.5e12.cm^{-2} respectively for different cell pitches. The V_{Pinch} in this study is defined at the voltage at which the rate of drop of capacitance falls below 2fF/μm.V. These points are shown in the CV curves, and are compared with the analytical value in Figure 3. As can be seen, the analytical values are in good agreement with simulation results.

B. Charge Imbalanced Super Junction Columns

An imbalance in P and N column charge causes lowering of the pinch-off voltage. For a given N column charge Q_N, the rate of decrease in V_{Pinch} depends on the polarity of the charge imbalance. For $Q'_P > Q_N$, which corresponds to a net increase in the column charge, the pinch of voltage has a lower drop off rate, and happens when the N column gets fully depleted. The lowering of the pinch off voltage happens due to incomplete depletion of the higher charge P column which supports lower voltage, as illustrated in figure 4. In this case, the pinch off voltage can be derived as:

$$V'_{Pinch} = 0.5 * E_{Max} * \left(\frac{W_N}{2} + \frac{W'_P}{2} \right) \quad (4)$$

Since the N column is fully depleted,

$$E_{Max} = \frac{q}{\varepsilon_s} * N_D * \frac{W_N}{2} = \frac{q * Q_N}{2 * \varepsilon_s} \quad (5)$$

$$W'_P = \frac{Q_N}{Q'_P} * W_P \quad (6)$$

Substituting (5) and (6) in (4), and defining $\delta Q = Q'_P - Q_N$

$$V_{Pinch} = \frac{q * Q_N}{8 * \varepsilon_s} * \left(W_{Cell} - W_P * \frac{\delta Q}{Q_N + \delta Q} \right) \quad (7)$$

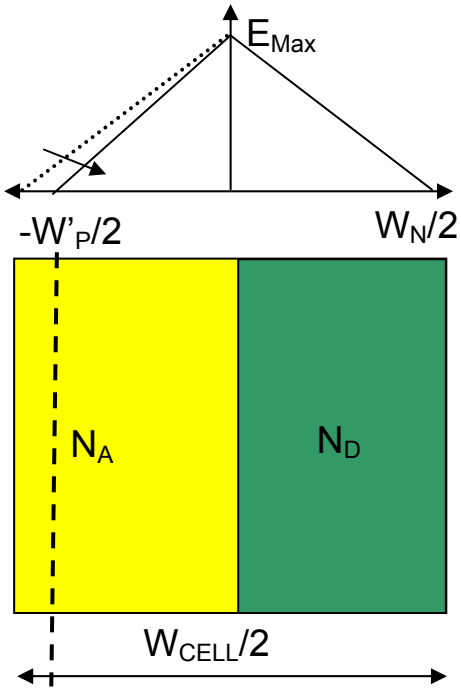


Figure 4. Electric field profile for $Q'_P > Q_N$ charge imbalanced Super Junction Columns at Pinch-off.

For the case $Q'_P < Q_N$, the V_{Pinch} drop off rate is higher. In this case, the lightly doped P column get depleted before the N column, and the lowering of the pinch off voltage happens from the lower P column charge, as well as the lower voltage supported by the N column due to charge imbalance. The analytical expression for Pinch off voltage is given by:

$$V'_{Pinch} = \frac{q * (Q_N - \delta Q)}{8 * \varepsilon_s} * \left(W_{Cell} - W_N * \frac{\delta Q}{Q_N} \right) \quad (8)$$

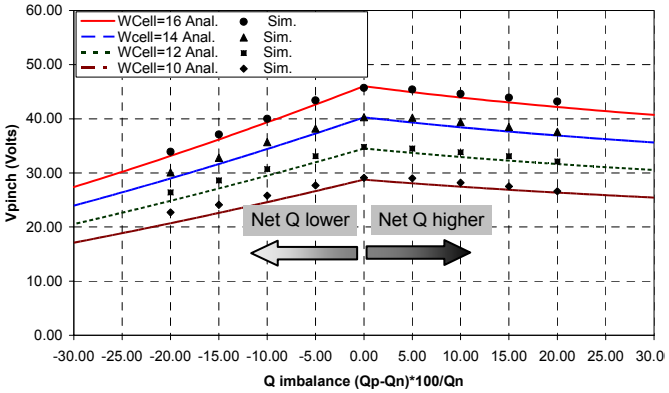


Figure 5. Comparison of Analytical & Simulated V_{Pinch} as a function of % column charge imbalance for Q_N=1.5e12cm^{-2}

In this case, $\delta Q = Q_N - Q'_P$. Figure 5 compares the simulated V'_{Pinch} for charge imbalanced P and N columns for Q_N=1.5e12.cm^{-2} with the analytical expressions, and shows a good match for various cell pitches. The P and N columns were chosen to be of equal width in this analysis.

In order to determine the magnitude of charge imbalance, the first step is to determine the conducting column charge Q_N. This can be done by measuring the $R_{DS,on}$ of the Super Junction MOSFET. Subsequently, charge imbalance can be determined by measuring the pinch off voltage and applying expressions (7) or (8) for $Q'_P < Q_N$ or $Q'_P > Q_N$ respectively. The polarity of charge imbalance can be determined by measuring C_{J0}, the junction capacitance at zero bias, which increases monotonically with the column charge, as shown in figure 6.

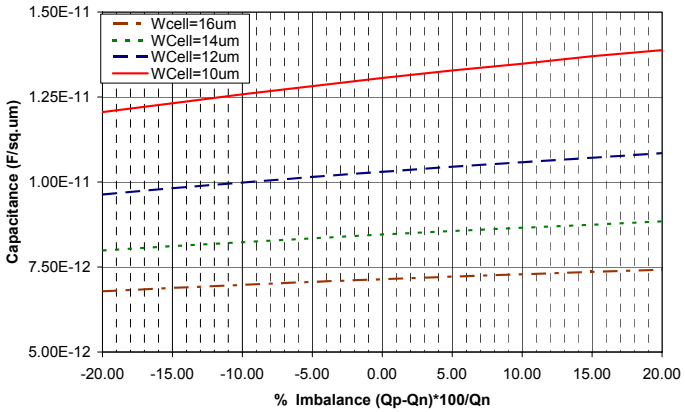


Figure 6. Simulated Zero Bias Junction Capacitance C_{J0} as a function of % column charge imbalance for Q_N=1.5e12cm^{-2}

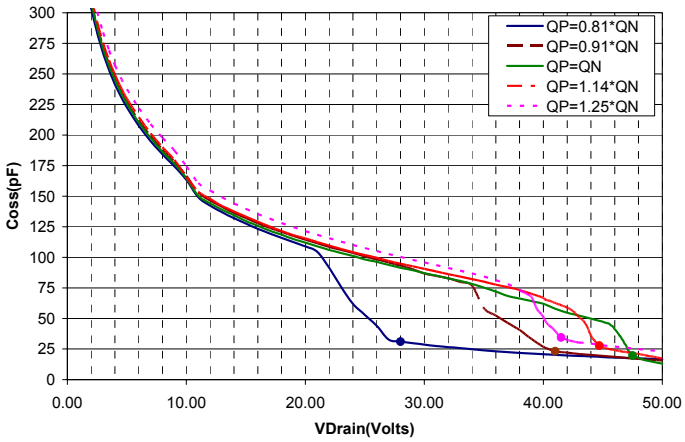


Figure 7. Measured C_{OSS} vs V_{DS} on 600V Super Junction MOSFETs

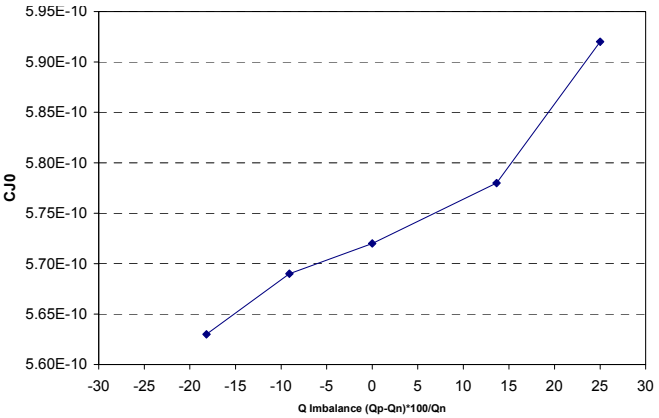


Figure 9. Measured C_{J0} vs P Column Dose on Fabricated 600V Super Junction MOSFETs

III. MEASUREMENT RESULTS

Figure 7 shows the measured CV on 600V SJ MOSFETs fabricated with a +/- 20% variation in the P column charge. Consistent with analysis, the Pinch off voltage peaks when the columns are charge balanced, and falls off at different rates for $Q'_P<Q_N$ and $Q'_P>Q_N$. Figure 8 compares the measured pinch off voltage with the analytical expression, and show excellent match for +/-10% charge imbalance. For charge imbalances larges than 10%, the drop off in the Capacitance with DC bias is less sharp, leading to inaccuracies in determining the exact pinch off voltage from the C-V curve. Figure 9 shows the measured C_{J0}, which increases with the P column charge and can be used to determine the polarity of the charge imbalance.

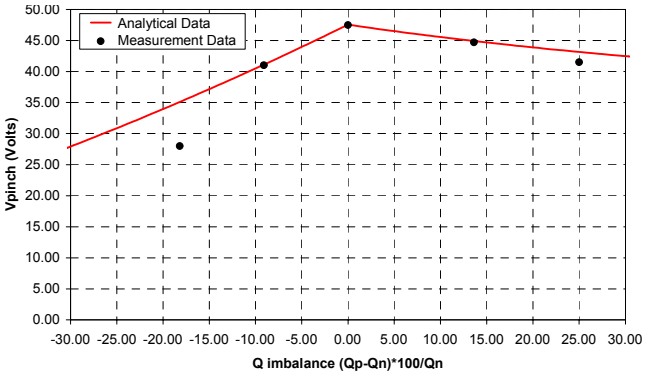


Figure 8. Comparison of Measured & Simulated V_{Pinch} as a function of % column charge imbalance

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